In the Specification:

Please amend the specification as follows:

Page 19, lines 3-16 (Abstract), kindly amend as follows:

~~An apparatus includes a field programmable gate array (FPGA). The FPGA includes a first FPGA tile, and the first FPGA tile includes a plurality of functional groups (FGs), a third set of routing conductors, in addition to a first set of routing conductors and a second set of routing conductors and a plurality of interface groups (IGs). The plurality of FGs are arranged in rows and columns with each of the FGs being configured to receive tertiary input signals as well as regular input signals, perform a logic operation, and generate regular output signals. The third set of routing conductors is coupled to the first set of output ports of the FGs and configured to receive signals, route signals within the first FPGA tile, and provide input signals to the third set of input ports of the FGs. The plurality of IGs surround the plurality of FGs such that one IG is positioned at each end of each row and column. Each of the IGs is coupled to the third set of routing conductors and configured to transfer signals from the third set of routing conductors to outside of the first FPGA tile.~~A method of accessing the testing means in a Field Programmable Gate Array ("FPGA") comprised of a plurality of functional groups ("FGs") comprising: inputting a function netlist defining a user circuit; compiling said function netlist; and generating a logic Built-In Self Test ("BIST") netlist; wherein said BIST netlist replaces all user registers with scan registers with a scan chain routed as the physical silicon scan chains.